REMARKS/ARGUMENTS

This is in response to an Office Action dated 08/03/2005.

Status

Claims 1-19 are pending

Claims 11-19 are withdrawn from consideration

Claims 1-10 are rejected

The Specification is objected to

The Drawings are accepted

Election/Restrictions

In the Response to Restriction Requirement dated 07/19/2005, Applicant has elected without traverse Invention of Group I (Claims 1-10) drawn to a device is acknowledged. Accordingly, claims 11-19 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 35 § 1.142(b) and MPEP § 821.03. Applicant has the right to file a divisional application covering the subject matter of the non-elected claims 11-19, drawn to a method.

Claims 11-19 are canceled herewith.

Information Disclosure Statement

This office acknowledges receipt of the following items from the applicant: Information Disclosure Statement (IDS) filed on 04/28/2004. The references cited on the PTOL 1449 form have been considered.

No response required.

PAGE 7/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

Specification

The disclosure is objected to because of the following informalities:

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

A new title is provided herewith, matching the scope of the invention to which the claims are directed.

Claim Rejections - 35 U.S.C. § 102

Claims 1-8 and 10 are rejected under 35 U.S.C. 102(b) as being anticipated by Hopper et al. (USP 6,518,646 hereinafter referred to as "Hopper").

Regarding **claims 1 and 2,** Hopper discloses in Fig. 2 and its corresponding texts as set forth in column 4, line 35-column 7, line 30, an interlevel dielectric layer 11 comprises:

a dielectric layer/a lower low-k dielectric layer 14; and

a dielectric film/a upper dielectric layer 16 atop the dielectric layer/the lower low-k dielectric layer.

However, the limitation "deposited under compressive stress" is taken to be a product by process limitation and consider non-limitation. In a product-by-process claim, it is the patentability of the claimed product and not of the recited process steps which must be established. Therefore, when the prior art discloses a product which reasonably appears to be identical with or only slightly different than the product claimed in a product-by process claim, a rejection based on sections 102 or 103 is fair.

The Patent Office is not equipped to manufacture products by a myriad of processes put before it and then obtain prior art product and make physical comparisons therewith. In re Brown, 173 USPQ 685 (CCPA 1972). Also, a product by process claim directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ I S at 17 (footnote 3). See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al.,

PAGE 8/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

218 USPQ 289, 292 (Fed. Cir. 1983); and particularly In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product gleaned' from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Regarding **claims 3 and 4,** Hopper discloses the dielectric layer/the lower low-k dielectric layer comprises an organosilicon glass (SOG) (col. 2, lines 18-33), or a SiCOH material (col. 5, line 19).

Regarding **claims 5 and 6,** Hopper discloses the dielectric layer/the lower low-k dielectric layer has a thickness of 500 -20,000 A/1000 - 15,000 A, and the dielectric film/the upper dielectric layer has a thickness of 200 - 2000 A/350 1000 A (col. 5, lines 40-61).

Regarding **claims 7 and 8,** Hopper discloses the dielectric film/the upper dielectric layer has a thickness which is 2% - 10% (lower range thickness of the dielectric film/the upper dielectric layer = 50 A ÷ lower range thickness of the dielectric layer/the lower low-k dielectric layer = 2000 A) 2.5% ~ 3% of the thickness of the dielectric layer/the lower low-k dielectric layer; and the dielectric film has a thickness which is approximately 3% of the thickness of the dielectric layer (col. 5, lines 40-61).

Regarding **claim 10,** Hopper discloses in Fig. 2 a dielectric cap 18 is deposited on the dielectric film/the upper dielectric layer.

Claim Rejections -35 USC § 103

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hopper et al. (USP 6,518,646 hereinafter referred to as "Hopper").

Hopper discloses the all claimed limitations except for the dielectric film has similar chemical composition to the dielectric layer, but has different morphology than the dielectric layer. It would have been obvious to one having ordinary skill in the art at the time of the invention was made to use the dielectric film having similar chemical composition to the dielectric layer, but having different morphology than the dielectric layer, since it has been held to be within the general skill of a worker in the art to select

PAGE 9/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

The Invention, Generally

The invention is generally directed to low-k interlevel dielectric layer (ILD) and method. An interlevel dielectric layer (ILD) comprises a low-k dielectric layer; and a low-k dielectric film, deposited under compressive stress, atop the dielectric layer. The dielectric layer comprises a low-k material, such as an organosilicon glass (OSG) or a SiCOH material. The dielectric film has a thickness, which is 2% - 10% of the thickness of the dielectric layer, has a similar chemical composition to the dielectric layer, but has a different morphology than the dielectric layer. The dielectric film is deposited under compressive stress, in situ, at or near the end of the dielectric layer deposition by altering a process that was used to deposit the low-k dielectric layer. (See Abstract)

Traversing the Rejection

Hopper (6,518,646) discloses semiconductor device with variable composition low-k inter-layer dielectric and method of making. Strong adhesion to doped low-k inter-layer dielectrics is provided by varying the composition of dopant near the surface layers of the inter-layer dielectric. The concentration of dopant is gradually increased from about zero atomic % at the interface between the inter-layer dielectric and semiconductor substrate to improve adhesion of the inter-layer dielectric to the semiconductor substrate. The concentration of dopant at the upper surface of the inter-layer dielectric is gradually decreased to about zero atomic % at the upper surface of the inter-layer dielectric film in order to improve adhesion of additional layers to the inter-layer dielectric. (See Abstract) The Examiner mainly cites Fig. 2 and its corresponding texts as set forth in column 4, line 35 - column 7, line 30, and additionally cites col. 2, lines 18-33 and col. 5, line 19, and col. 5, lines 40-61.

The Present Invention, In Greater Detail

The present invention is illustrated in FIGs. 1 and 2 which are described in the specification, as follows.

PAGE 10/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

FIG. 1 is a cross-sectional view of a relevant portion of a semiconductor device - namely, an interlevel dielectric layer (ILD) - illustrating a first step in a process of forming the ILD, according to the invention.

FIG 2 is a cross-sectional view illustrating further steps in the process, according to the invention.

FIG. 1 is a cross-sectional view of a relevant portion of a semiconductor device - namely, an interlevel dielectric layer (ILD) 100 - formed according to the techniques of the present invention. The ILD 100 comprises a low-k primary dielectric layer 102 and a compressive low-k dielectric film 104 deposited atop the primary dielectric layer 102. (The primary dielectric layer 102 can be two layers, in a dual damascene process.) As is known in the art, the primary dielectric layer 102 is deposited on the surface of a semiconductor wafer (not shown).

The compressive low-k dielectric film 104 is deposited to serve as a hard mask for the primary dielectric layer 102. In an embodiment of the invention, the compressive low-k dielectric film 104 is deposited, at or near the end of the primary dielectric layer 102 deposition. The deposition is accomplished by altering the process conditions (e.g., gas flow, power, pressure, bias) which were being used to deposit the primary dielectric layer 102 to yield a film 104 under compressive stress while maintaining a low dielectric constant. The film 104 also possesses properties that enable it to function as a polish stop layer during copper chemical mechanical polishing (CMP).

FIG. 2 is a cross-sectional view of a further step in the process, illustrating that a via 106 and a trench 108 have been formed in the ILD 100, and the via 106 and trench 108 have been filled with damascene copper (Cu) 110. The process of forming damascene copper interconnects in an ILD is well known, and the steps involved (e.g., barrier, liner, copper seed, plate) are omitted, for illustrative clarity.

The resulting interconnect structure (ILD with copper) is subjected to chemical mechanical polishing (CMP), which planarizes the top surface of the interconnect structure and also thins

PAGE 11/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

compressive low-k dielectric film, designated 104' in this figure. Following the steps of forming damascene copper and subjecting it to CMP, a dielectric cap 112, such as nitrogen-doped silicon carbide or Si-N-C-H (NBLOk) is deposited on the resulting structure. The dielectric cap 112 should also be under compressive stress.

The primary dielectric layer 102 has a thickness of 500 - 20,000 Å (Angstroms) and preferably between 1000 - 15,000 Å.. The primary ILD layer 102 is a low-k material such a SiCOH material, such as Black Diamond™, an organosilicon glass (OSG).

The compressive film 104 has a thickness of 200 - 2000 Å and preferably between 350 - 1000 Å. The compressive film 104 has similar chemical composition to the primary dielectric layer 102, but different morphology (mechanical properties).

Being denser than the primary dielectric layer 102, the compressive film 104 has a higher dielectric constant than the primary dielectric layer 102. Therefore, it is desirable to keep the compressive film 104 as thin as possible to reap the desired mechanical benefits without unnecessarily sacrificing the overall low-k of the ILD 100. For example, the compressive film 104 has a thickness which is 2% - 10% and preferably about 3% of the thickness of the primary dielectric layer 102. For example, the primary dielectric layer 102 has a thickness of 10,000 Å, and the compressive film has a thickness of 500 Å.

The dielectric cap 112 has a chemical composition SiNXCYHZ (NBLOk) and has a thickness of 100 - 1000 Å and preferably about 250 - 500 Å .

Hopper, more particularly

The following are some illustrative excerpts (highlights) from Hopper.

As shown in FIG. 1, semiconductor device 10 is formed by depositing a lower layer of a doped dielectric 14 on semiconductor substrate 12. The doped dielectric includes carbon-doped (or organic-doped) silica glasses, such as SiCOH, and fluorine-doped glasses such as fluorine-doped silica glass (FSG) or in particular fluorine-doped tetraethylorthosilicate (FTEOS). (paragraph starting at column 4, line 66)

The SiCOH ILD (14) ... is formed using a plasma enhanced chemical vapor deposition technique (PECVD). (column 5, lines 18-20)

The ILD lower layer 14 is deposited to a predetermined thickness, typically about 2000 Å to about 1.2 µm. After the predetermined thickness of the ILD lower layer 14 is reached, TEOS is introduced into the reactor at a flow rate of 500 to about 3000 sccm. The flow rate of the trimethylsilane is gradually decreased while the flow rate of the TEOS is gradually increased to form the ILD upper layer 16, as shown in FIG. 2, wherein the concentration of dopant in the dielectric film is gradually reduced across the thickness of the upper layer. The flow rates of the precursor gases are varied so that by the time upper surface 17 of upper layer 16 is formed the trimethylsilane flow is reduced to 0 sccm. The concentration of the carbon dopant is reduced from the concentration in the ILD lower layer 14 at the lower layer/upper layer interface to about 0 atomic % at the upper surface of the upper layer. In other words, the surface of the upper layer of the ILD is approximately pure USG. The thickness of the ILD upper layer 16 is about 50 Å to about 500 Å preferably about 100 Å to about 200 Å. The upper surface 17 of the ILD upper layer 16, which contains approximately 0 atomic % of dopant can range up to about 50 Å thick. The upper layer 16 and lower layer 14 form ILD 11. (column 5, lines 40-62)

Contrasting the Invention with Hopper

In Hopper, the purpose is is to provide a layer for improving adhesion of two layers, one above, one below. ("The SiO2 -like surface of upper layer 16 provides strong adhesion for subsequently deposited additional layers 18." Hopper, column 6, lines 37-38)

The present invention is directed to the structure of an ILD. The materials are similar to those of Hopper, but it is not for adhesion, rather is for capping to prevent moisture.

Hopper discloses depositing a first layer (14). Then, the process is gradually modified so that a subsequent layer (16) has a gradually reducing (from non-zero to zero) concentration of dopant gradient. The upper layer 16 and lower layer 14 form ILD 11.

PAGE 13/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

Hopper's first layer (14) has a thickness of 2000 Å - 1.2 µm (2000 - 12,000 Å). Hopper's second layer (16) has a thickness of about 50 Å to about 500 Å preferably about 100 Å to about 200 Å.

Crunching the numbers, Hopper's second layer has a thickness (50-500) which is in the range of 0.4% (50/12000 Å) -to- 25% (500/2000 Å) of the thickness (2000-12000 Å) first layer.

Compare claim 7. The interlevel dielectric layer, according to claim 1, wherein the dielectric film has a thickness which is 2% - 10% of the thickness of the dielectric layer.

The present invention is directed to an interlevel dielectric layer (ILD) comprising a low-k dielectric layer; and a low-k dielectric film, deposited under compressive stress atop the dielectric layer. The dielectric layer comprises a low-k material, such as an organosilicon glass (OSG) or a SiCOH material. The dielectric film has a thickness of 2% - 10% of the thickness of the dielectric layer, a similar chemical composition to the dielectric layer, but a different morphology than the dielectric layer. (page 5, Summary of the Invention, second full paragraph)

In the present invention, the primary (lower) dielectric layer 102 has a thickness of 500 - 20,000 Å (Angstroms) and preferably between greater than 12000 - 20,000 Å. This range has been found to be useful because the power distributor or interconnects operate better when they are thicker. This is different from Hopper.

In the present invention, the second layer - the compressive film 104 has a thickness of 200 - 2000 Å and preferably between 1000 - 2000 Å. This range has been found to work in practice. The compressive film 104 has similar chemical composition to the primary dielectric layer 102, but different morphology (mechanical properties). The compressive film 104 is denser than the primary dielectric layer 102. This is different than Hopper.

First of all, **Claim 1** is amended herewith to include the limitation of **claim 9** (canceled) and emphasize the different morphology of the second layer, as discussed above.

Newly-presented **claim 20** is directed to the compressive film 104 is denser than the primary

PAGE 14/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

dielectric layer 102, as discussed above. Applicant is generally amenable to incorporating this limitation into the main claim, if necessary, to obtain allowance of claim 1.

Comparing the numbers:

	Hopper discloses	Present Invention discloses
upper layer	50 - 500	200 - 2000, preferably 350 - 1000
lower layer	2000 - 12000	500 - 20000, preferably 1000 - 15000

Hopper ***does not*** disclose, and the Present Invention ***does*** disclose:

- upper layer (film): from greater than 1000 up to 2000
- lower layer (layer): from greater than 12000 to 20000

Newly-presented independent **claim 21** is directed to these ranges.

Newly-presented dependent **claims 22 - 27** are similar to the original claims, as filed. (22 - 2; 23 - 3; 24 - 4; 25 - 9; 26 - 10; 27 - 20)

Claim Count

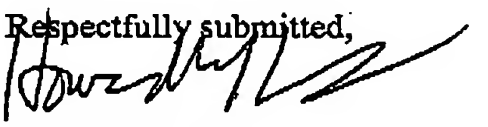
17 total claims (1-8, 10, 20; 21-27)

2 independent claims (1,21)

Conclusion

Applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,



Howard M. Cohn
Registration No. 25,808

Howard M. Cohn
21625 Chagrin Blvd. Suite 220
Cleveland, OH 44122
Voice (216) 752-0955
Fax (216) 752-0957

PAGE 15/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08

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PAGE 16/16 * RCVD AT 11/3/2005 3:38:59 PM [Eastern Standard Time] * SVR:USPTO-EFXRF-6/34 * DNIS:2738300 * CSID:216 752 0957 * DURATION (mm-ss):05-08